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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
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ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/763,308	NARASIMHA ET AL.	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-9,12-14 and 17-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-9,12-14 and 17-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-4, 6-9, 12-14 and 17-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claimed limitations of forming first silicide regions having a first silicide thickness in the substrate as well as atop a surface of the gate region, wherein said first silicide regions have a lateral thickness from about 2 to about 15 nm which lowers external resistance of said device, as recited in claim 1, are unclear as to which element is atop a surface of the gate region and whether the lateral thickness of said first silicide regions is the total lateral thickness of all of said first silicide regions or it is the lateral thickness of each silicide region.

The claimed limitations of a first silicide thickness and a second silicide regions have a thickness that is greater than the first silicide thickness, as recited in claim 1, are unclear to whether applicant refers to vertical thicknesses or lateral thicknesses.

The claimed limitations of first spacers width and second spacers width, as recited in claims 6-9, respectively, are unclear as to whether applicant refers the width of one spacer or the width of the combined spacers.

The claimed limitation of a thickness, as recited in claim 17, is unclear as to which thickness applicant refers.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 6-9, 12-14 and 17-19, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Son (6,063,681).

Regarding claim 1, Son teaches in figures 3A-H a method for forming a low resistance MOSFET device comprising the steps of:

forming a gate region (25) atop a surface of substrate (21);

forming first spacers (26) having a first spacer width on sidewalls of the gate region (25);

forming first silicide regions (29) having a first silicide thickness in the substrate (21) as well as atop a surface of the gate region (25), wherein said first silicide regions have a thickness from about 10 to about 20 nm which lowers external resistance of said device;

forming second spacers (31) having a second width greater than the first spacer (26) width (figure 3H) on the substrate (21), wherein the second spacers (31) protect the first silicide region (29) in the substrate (21); and

forming second silicide regions (33) in the substrate (21) and atop a surface of the gate region (25), wherein the second silicide regions have a thickness that is greater than the first silicide thickness.

Son does not explicitly state that said first silicide regions have a lateral thickness from about 2 to about 15 nm.

Son teaches said first silicide regions have a thickness from about 10 to about 20 nm (100 – 200 Angstroms, column 3, lines 58-63).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use first silicide regions having a lateral thickness from about 2 to about 15 nm in Son's device in order to adjust and optimize the resistance of the device with respect to the contact resistance of the device.

Regarding claim 6, Son differs from the claimed invention by not showing the first spacers width is from about 5nm to about 20 nm. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the first spacer width is from about 5nm to about 20 nm in Son's device in order to provide better protection for the gate electrode. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 7, Son differs from the claimed invention by not showing the first spacers width is from about 7 nm to about 15 nm. It would have been obvious to one

having ordinary skill in the art at the time the invention was made for the first spacer width is from about 7 nm to about 15 nm in Son's device in order to provide better protection to the gate electrode. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 8, Son differs from the claimed invention by not showing the second spacers width is from about 20 nm to about 90 nm. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the second spacers width is from about 20 nm to about 90 nm in Son's device in order to provide better protection to the gate electrode. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 9, Son differs from the claimed invention by not showing the second spacers width is from about 30 nm to about 70 nm. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the second spacers width is from about 30 nm to about 70 nm in Son's device in order to provide better protection to the gate electrode. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 12, Son shows forming of the first silicide region (29) comprises depositing a first metal layer (28) upon an exposed surface of the substrate (21) and annealing (column 3, lines 58-62).

Regarding claim 13, Son differs from the claimed invention by not showing the first metal layer has a thickness from about 2 nm to about 7 nm. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the first metal layer has a thickness from about 2 nm to about 7 nm in order to increase the conductivity of metal layer. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 14, Son teaches the first metal layer 28 comprises Ti (column 4, lines 5-6).

Regarding Claim 17, Son teaches a thickness 29 is between 10 – 20 nm (100-200 Angstroms; column 3, lines 58-62), which is in the range (5 –12 nm) of the claimed invention.

Regarding claims 18-19, Son teaches the first silicide region 29 is formed in the substrate 21 having a channel region beneath the gate region, but differs from the claimed invention by not showing the distance between the first silicide region and the

channel region is from about 2 nm to about 15 nm. It would have been obvious to one having ordinary skill in the art at the time the invention was made for form the distance between the first silicide region and the channel region from about 2 nm to about 15 nm in Son's device in order to increase the speed of the device. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Son in view of Kim et al. (6,313,020)

Son teaches substantially the entire claimed structure, as applied to claim 1 above, except pre-doping the gate region. Kim et al. teach forming of the gate region comprising predoping process (column 1, lines 26-34). It would have been obvious to one having ordinary skill in the art at the time the invention was made to pre-dope the gate region of Son's device in order to improve the level of the electrons in the gate region.

Regarding claim 3, the combined device shows the pre-doping is preformed by ion implantation of a type III-A element (Kim et al.; Boron is III-A element; column 1, lines 30-34).

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Son and Kim et al., as applied to claims 1-3 above, and further in view of Krishnan et al. (6,399,452).

Son and Kim et al. teach substantially the entire claimed structure, as applied to claims 1-3 above, except pre-doping via ion implantation of phosphorus into the gate region. Krishnan et al. teach pre-doping by implantation of phosphorus into the gate (column 2, lines 42-53). It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Krishnan et al. into the method taught by Son and Kim et al. in order to improve the level of the electrons in the gate region.

Response to Arguments

Applicant argues that Son teaches in column 3, line 26 that the thickness of the first silicide region is from about 200 to about 400 Angstroms, i.e. 20 to 40 nm, and not from about 2 to about 15 nm, as required by claim 1.

Son does not teach in column 3, line 26 that the thickness of the first silicide regions is from about 200 to about 400 Angstroms. Son teaches in column 3, lines 23-24 that the first silicide region is formed to a depth of about 200 to about 400 Angstroms. However, claim 1 requires that the first silicide regions have a lateral thickness from about 2 to about 15 nm. Clearly, depth is not lateral thickness.

Therefore, Son does not teach that the lateral thickness of the first silicide regions is from about 200 to about 400 Angstroms, as argued by applicant.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Loke can be reached on 571-272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
9/20/05

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